GAU 2818

PATENTS

03.01.02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. 01-44)

In the application of:

Sunil Mehta and Fabiano Fontana

Serial No. 09/991,245

Filed: November 14, 2001

For: Zero-Power Programmable Memory Cell

Examiner:

Group Unit: 2818

Asst. Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

TRANSMITTAL LETTER

In regard to the above identified application:

1. We are transmitting herewith the attached Information Disclosure Statement and copies of references cited; Form PTO-1449; and postcard

2. With respect to additional fees:

   X A. No additional fee is required.

   ____ B. Attached is a check in the amount of $____.

3. CERTIFICATE OF MAILING UNDER 37 CFR § 1.8: The undersigned hereby certifies that this Transmittal Letter and the paper, as described in paragraph 1 hereinabove, are being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231 on this 17th day of December, 2001.

By Monica H. Choi
Monica H. Choi
Reg. No. 41,671

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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.97 - 1.98, the Applicants wish to make the following documents of record in the above-identified application. This Information Disclosure Statement is in compliance with the duty of candor as set forth in 37 C.F.R. § 1.56. Copies of the documents cited below are enclosed. These documents are also listed on the enclosed PTO Form 1449.

In the judgment of the undersigned, portions of the listed documents may be material to the patentability of the presently pending claim. However, the documents have not been reviewed in sufficient detail to make any other representation and, in particular, no representation is intended as to the relative importance of any portion of the documents. This

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statement is not a representation that the listed documents have effective dates early enough to be "prior art" within the meaning of 35 U.S.C. § 102 or § 103.

List of Cited References

I. Patents

Patent No.	Title	Inventors
4, 829,203	Integrated Programmable Bit Circuit with Minimal Power Requirement	Ashmore, Jr.
4,862,019	Single-Level Poly Programmable Bit Circuit	Ashmore, Jr.
4,866,307	Integrated Programmable Bit Circuit Using Single-Level Poly Construction	Ashmore, Jr.
4,885,719	Improved Logic Cell Array using CMOS E^2 PROM Cells	Brahmbhatt
4,924,278	EEPROM Using a Merged Source and Control Gate	Logie
5,270,587	CMOS Logic Cell for High-Speed Zero-Power Programmable Array Logic Devices	Zagar
6,028,789	Zero-Power CMOS Non-Volatile Memory Cell having an Avalanche Injection Element	Mehta et al.

II. Other

Title	Serial No.	Filing Date
Wide Input Programmable Logic System and Method (to Ravindar M. Lall)	09/704,487	11/2/2000

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Respectfully Submitted,

Date: December 17, 2001

By: Monica H. Choi

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CERTIFICATE OF MAILING

The undersigned hereby certifies that the foregoing INFORMATION DISCLOSURE STATEMENT is being deposited in the United States Postal Service, as first class mail, postage prepaid, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on this 17th day of December, 2001.

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